Novel Low Capacitance Sidewall Elevated Drain Dynamic Threshold Voltage MOSFET (LCSED) for Ultra Low Power Dual Gate CMOS Technology

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ABSTRACT

We have developed a novel high speed dynamic threshold voltage MOSFET named LCSED for ultra low power operation. This was realized using sidewall elevated drain. The LCSED achieved the following excellent characteristics as compared to the Bulk-DTMOS which we proposed before: 60% reduced occupation area; 65% reduced junction capacitance; 67% reduced forward leakage current between shallow-well and source/drain; lower transistor series resistance; smaller short channel effect; higher drive current. These effects realize ultra low power high speed operation.

INTRODUCTION

For battery operating portable electronic equipment, reduction of power dissipation in CMOS-LSI has been the most important subject in order to realize long life mobile operation. The power dissipation in CMOS circuit is proportional to the square of power supply voltage and load capacitance. Therefore, reduction of power supply voltage is the most effective method to extend battery life. However, the extreme scaling down of power supply voltage causes reduction in gate overdrive and operation speed, because of a difficulty of threshold voltage reduction due to the extreme increase of standby leakage current. To achieve lower power supply voltage operation with low subthreshold leakage and relatively high drive current, a dynamic threshold voltage MOSFET (DT-MOS) was proposed using SOI wafer (SOI DT-MOS)[1] or bulk wafer (B-DTMOS)[2]. This MOSFET provides low threshold voltage when the device is turned-on, and high threshold voltage when the device is turned-off. This device was realized by the gate to body or well tie structure. However, in SOI DT-MOS , long RC delay of gate to body signal transmission due to heavy resistance of the body layer was the most severe issues for high speed operation. In the B-DTMOS, RC delay problem was solved by low resistance individual shallow well structure separated using trench isolation and deep well[2]. However, large junction capacitance due to the mirror effect in drain junction degraded the low power operation. To overcome this problem, we propose a low capacitance sidewall elevated drain dynamic threshold voltage MOSFET (LCSED-DTMOS) implemented on bulk wafer. In LCSED-DTMOS sidewall elevated drain structure was applied to the bulk dynamic threshold MOSFET (B-DTMOS) to reduce junction capacitance.

RESULTS AND DISCUSSION

A. LCSED Structure

The LCSED structure has an ultimately narrow source and drain width (2/3L; L = gate length) due to the enhancement of the effective surface area by the elevated structure, as shown in Fig.1. Figure 2 shows a cross section SEM image of the LCSED. In this structure, the sidewall elevated source and drain was fabricated by poly-silicon deposition using an oxygen free Load-Lock LPCVD system[3] and subsequent etching-back after gate formation. Although the junction area was very narrow, the convex top surface of the poly-silicon sidewall enable us to achieve enough contact area between source and drain electrodes and metal line. Figure 3 shows a schematic top view of LCSED-DTMOS. The poly-silicon of the gate electrode at the portion of shallow-well connection was removed in order to connect the gate with shallow-well. The poly-silicon sidewall which surrounded the gate electrode was partially removed at the each end of the gate to separate the source and drain region. The gate to shallow-well connection was realized using "simultaneous fabrication of the source, drain and gate salicide, and gate to shallow well connection (SSS-C)[2]" process. In this process, the gate electrode was connected to the shallow-well as a matter of course by the silicide film when source/drain and gate silicidation were carried out.

One of the disadvantages of B-DTMOS was large occupation area in the case of multiple step serial connection of transistors. Figure 4 shows a ratio of the occupation area of serially connected LCSED, B-DTMOS and conventional MOSFET to that of the single conventional MOSFET as a function of connected number. The B-DTMOS which we proposed before needed larger occupation area than that of the conventional MOSFET due to separating the shallow-well in each transistor and connecting with each intermediate node by metal line. In the LCSED structure, 60% reduced occupation area compared with the B-DTMOS was realized using small junction area and local interconnection by elevated drain. Furthermore, below the 5 connected transistors, the occupation area of the LCSED was smaller than that of the conventional MOSFET.

B. Extra Parasitic Capacitance and Forward Current in DTMOS

The B-DTMOS has extra parasitic junction capacitance component (C_{DF}: drain / shallow-well junction capacitance for zero to forward bias due to mirror effect, C_S: source / shallow-well junction capacitance, C_{DEP}: depletion layer / shallow-well

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