

A 1-GHz Bipolar Class-AB Operational Amplifier with Multipath Nested Miller Compensation for 76-dB Gain

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Abstract—A 1-GHz operational amplifier with a gain of 76 dB while driving a 50- Ω load is presented. The equivalent input noise voltage is as low as 1.2 nV/ $\sqrt{\text{Hz}}$. This combination of extremely high bandwidth, high gain, and low noise is the result of a three-stage all-n-p-n topology combined with a multipath nested Miller compensation. Using 10-GHz f_T n-p-n transistors, the realizable bandwidth could be of the order of 2–3 GHz. However, bond-wire inductances restrict the useful bandwidth to 1 GHz. The amplifier occupies an active area of 0.26 mm² and has been realized in the bipolar part of a 1- μm BiCMOS process.

Index Terms—Analog integrated circuits, bipolar integrated circuits, frequency compensation, HF amplifiers, operational amplifiers.

I. INTRODUCTION

TRADITIONALLY, wideband amplifiers consist either of stages with local feedback, which reduce accuracy, or use feedforward techniques that introduce pole-zero doublets, which deteriorate the settling behavior [1]. Recently reported multistage compensation techniques, such as multipath nested Miller compensation [2], allow frequency compensation of cascaded gain stages with minimal reduction in bandwidth compared to single-stage amplifiers. This enables amplifiers to combine high gain and high bandwidth. This paper describes how multipath nested Miller compensation makes the realization of a general-purpose high-gain 1-GHz operational amplifier possible.

To obtain the highest possible bandwidth, only the device with the highest transit frequency, the n-p-n transistor, should be applied in the high-frequency signal path. Even in modern complementary processes, the n-p-n is a factor three faster than its p-n-p counterpart. Because of the fundamental difference in mobility of electrons and holes, this will not change in the future. Therefore, very wideband amplifiers should exploit an all-n-p-n topology [3]. For low frequencies, however, p-n-p transistors can be used. They are especially useful for obtaining the necessary dc levelshifts between n-p-n stages. A basic topology of a two-stage amplifier is shown in Fig. 1. The two-stage opamp has a gain only of the order of 40 dB

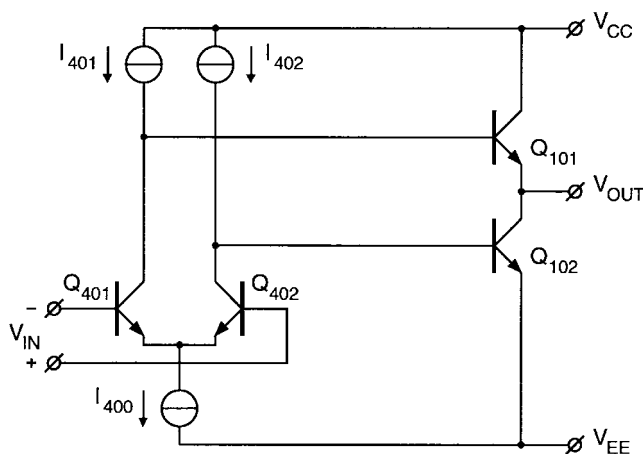


Fig. 1. Basic two-stage all-n-p-n topology.

when driving 50 Ω . Darlington transistors cannot be allowed in the output stage at extremely high bandwidths. Therefore, a third stage is necessary in combination with multipath nested Miller compensation. A theoretical elaboration of the multipath nested Miller compensation for low-ohmic loads and very high frequencies is presented in this paper.

The paper starts by examining the two-stage all-n-p-n topology in Section II. In Section III, the implementation of the all-n-p-n topology in a three-stage circuit using multipath nested Miller compensation is discussed. The complete circuit, the realization of the opamp, and the measurement results are presented in Section IV. Special attention is paid to the packaging and bonding of the amplifier. Finally, in Section V the conclusions are drawn.

II. TWO-STAGE ALL-n-p-n TOPOLOGY

A. Principle of Operation

A simplified schematic of a two-stage all-n-p-n opamp is shown in Fig. 1. It consists of an n-p-n input stage Q_{401} , Q_{402} and an n-p-n output stage Q_{101} , Q_{102} . Apart from the fact that only n-p-n transistors are used, the high-frequency behavior benefits from the very simple topology. Because the output stage consists of a follower Q_{101} and an inverter Q_{102} , the output stage can be directly driven by the differential input stage Q_{401} , Q_{402} without a mirror, which would have added

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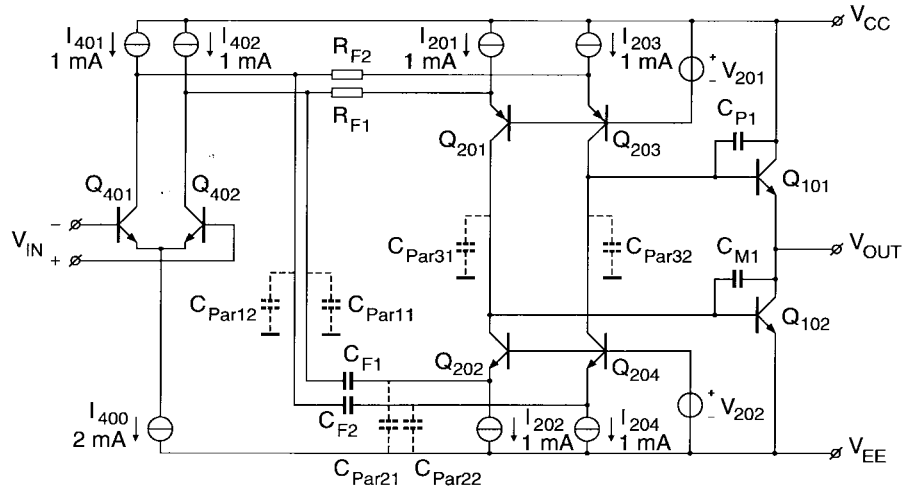


Fig. 2. Two-stage all-n-p-n opamp with level shift.

delay and parasitics. A practical implementation, however, gives rise to three main problems.

- 1) The common-mode input voltage of a general-purpose building block like an opamp should be independent of the biasing voltages of the output stage and the output voltage. To achieve this, a level-shift circuit between input stage and output stage is necessary. For the sake of good high-frequency behavior, the level shift should not introduce much delay and parasitic capacitance.
- 2) The output stage is asymmetric, with one output transistor being connected as a follower and the other output transistor as an inverter. To achieve good signal behavior, the push and pull output transistors should be balanced.
- 3) To be able to deliver sufficient output current without consuming a lot of quiescent current, the output stage should be biased in class AB. The class-AB control circuit should prevent cutoff of the output transistors and should not interfere with the signal path, in order to prevent delay and distortion.

B. Level Shift

To realize a wideband level shift, p-n-p cascodes Q_{201} , Q_{203} for low-frequency signals can be combined with n-p-n cascodes Q_{202} , Q_{204} for high-frequency signals, when we split the input signal by RC all-pass networks R_{F1} , C_{F1} and R_{F2} , C_{F2} as shown in Fig. 2. If the turnover frequency $f_{TO} = 1/R_{F1}C_{F1}$ is much lower than the transit frequency of the p-n-p transistor, the response of the circuit is flat up to the transit frequency of the n-p-n transistor [3] without pole-zero doublets. Unfortunately, several nonidealities influence the behavior of the level shift. For low frequencies, the transfer function is attenuated by the current gain of the p-

n-p transistor which is much lower than the current gain of the n-p-n transistor. For high frequencies, the transfer function is influenced by parasitic capacitances C_{Par11} – C_{Par32} , which are shown in Fig. 2. C_{Par11} and C_{Par12} attenuate the high-frequency transfer function. C_{Par21} and C_{Par22} are connected across the base-emitter capacitance of Q_{202} and Q_{204} , and thus reduce the bandwidth. C_{Par31} and C_{Par32} load the output stage.

C. Output Stage Balancing

The output transistors with their parasitics are shown in Fig. 3. Their nature is completely different because one is connected as a follower and the other as an inverter. However, it is possible to make the transfer function of the output transistors equal by making the capacitance across the base-collector junctions equal by adjusting C_{P1} , assuming the output transistors are driven by ideal current sources [3]. When we perform a detailed calculation, the transfer function from input voltage V_{in} to output voltage V_{out} of the follower is found as shown below in (1) where

- j complex unit;
- ω frequency;
- g_1 transconductance of the output transistors;
- g_2 transconductance of the input stage;
- β_F current gain of the output transistors;
- R_L load resistance;
- r_{be} small-signal base-emitter resistance of the output transistors;
- C_{be} base-emitter capacitance of the output transistors;
- C_L load capacitance.

C_{P1} also includes the base-collector capacitance C_{bc} and C_{Par31} . The transfer function of the inverter is found as shown

$$\frac{V_{out}}{V_{in}} = \frac{g_2 \beta_F R_L \left(1 + j\omega \frac{C_{be}}{g_1} \right)}{1 + j\omega (r_{be} C_{be} + R_L C_L + r_{be} C_{P1} + R_L C_{P1} + \beta_F R_L C_{P1}) + (j\omega)^2 r_{be} R_L (C_{be} C_L + C_{be} C_{P1} + C_L C_{P1})} \quad (1)$$