1. General Description

VD1400-GOB is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 7” active area with 1264 x 1680 pixels, the display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

2. Feature

- High contrast reflective/electrophoretic technology
- Carta 1300 with FastGLR and Eclipse
- 1264 x 1680 resolution and Glass backplane
- Ultra-wide viewing angle
- Low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape and portrait mode
- CTM Front Light, Warm and Cool color
- Capacitive touch of two ITO with finger and stylus writing support
- Cover with Anti-Glare film

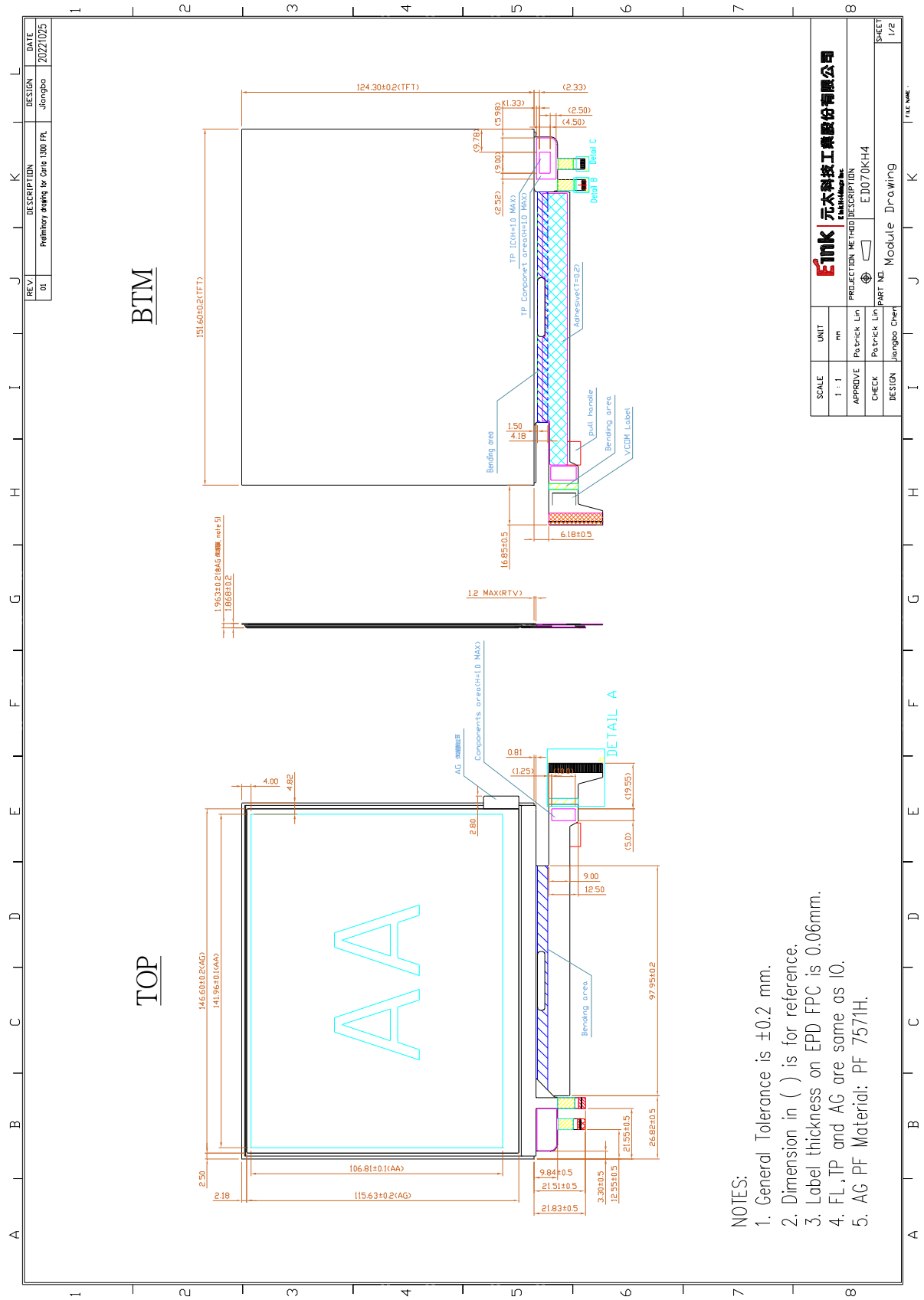
3. Mechanical Specifications

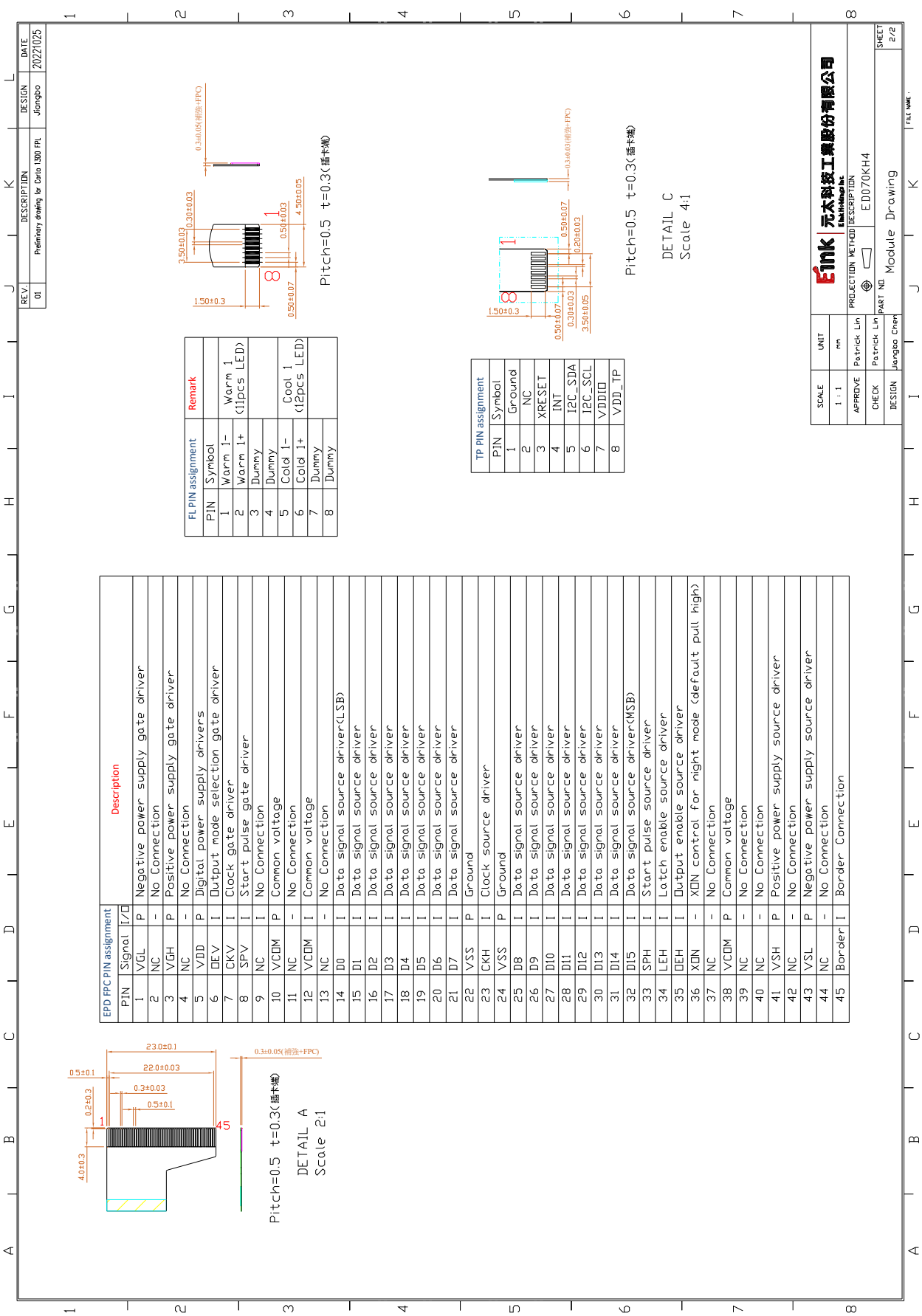
Parameter	Specifications	Unit	Remark
Screen Size	7 (3 : 4)	Inch	
Display Resolution	1264(H) × 1680(V)	Pixel	300 PPI
Active Area	141.96(H) x 106.808(V)	mm	
Pixel Pitch	0.0845(H) × 0.0845(V)	mm	
Pixel Configuration	Square		
Outline Dimension	151.6 x 124.3 x 1.87	mm	
Module Weight	61.97 ± 2	g	
Number of Gray	16 Gray Level (monochrome)		
Display operating mode	Reflective mode		
Surface treatment	haze 11% +/-3%, hardness >=3H”		3H Hardness, module only

3.1 Surface Protective Film

Model Name	Peeling Force (Adhesion to AG)
YHM protective film, 7-inch	25 ± 15 (gf/25mm)

4. Mechanical Drawing





REV.	DESCRIPTION	DESIGN	DATE
01	Preliminary drawing for Carta 1300 FPL	Jiangbo	20221025

EPD FPC PIN assignment

PIN	Signal	I/O	Description
1	VGL	P	Negative power supply gate driver
2	NC	-	No Connection
3	VGH	P	Positive power supply gate driver
4	NC	-	No Connection
5	VDD	P	Digital power supply drivers
6	OEV	I	Output mode selection gate driver
7	CKV	I	Clock gate driver
8	SPV	I	Start pulse gate driver
9	NC	I	No Connection
10	VCOM	P	Common voltage
11	NC	-	No Connection
12	VCOM	I	Common voltage
13	NC	-	No Connection
14	D0	I	Data signal source driver(LSB)
15	D1	I	Data signal source driver
16	D2	I	Data signal source driver
17	D3	I	Data signal source driver
18	D4	I	Data signal source driver
19	D5	I	Data signal source driver
20	D6	I	Data signal source driver
21	D7	I	Data signal source driver
22	VSS	P	Ground
23	CKH	I	Clock source driver
24	VSS	P	Ground
25	D8	I	Data signal source driver
26	D9	I	Data signal source driver
27	D10	I	Data signal source driver
28	D11	I	Data signal source driver
29	D12	I	Data signal source driver
30	D13	I	Data signal source driver
31	D14	I	Data signal source driver
32	D15	I	Data signal source driver(MSB)
33	SPH	I	Start pulse source driver
34	LEH	I	Latch enable source driver
35	OEH	I	Output enable source driver
36	XON	-	XON control for night mode (default pull high)
37	NC	-	No Connection
38	VCOM	P	Common voltage
39	NC	-	No Connection
40	NC	-	No Connection
41	VSH	P	Positive power supply source driver
42	NC	-	No Connection
43	VSL	P	Negative power supply source driver
44	NC	-	No Connection
45	Border	I	Border Connection

FL PIN assignment

PIN	Symbol	Remark
1	Warm 1-	Warm 1 (11pcs LED)
2	Warm 1+	
3	Dummy	
4	Dummy	
5	Cold 1-	Cool 1 (12pcs LED)
6	Cold 1+	
7	Dummy	
8	Dummy	

TP PIN assignment

PIN	Symbol
1	Ground
2	NC
3	XRESET
4	INT
5	I2C_SDA
6	I2C_SCL
7	VDDIO
8	VDD_TP

SCALE	UNIT	E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.	
1 : 1	mm	PROJECTION METHOD	DESCRIPTION ED070KH4
APPRIVE	Patrick Lin		
CHECK	Patrick Lin	PART NO	Module Drawing
DESIGN	Jiangbo Chen		SHEET 2/2

5. Input / Output Interface

5.1 Pin Assignment

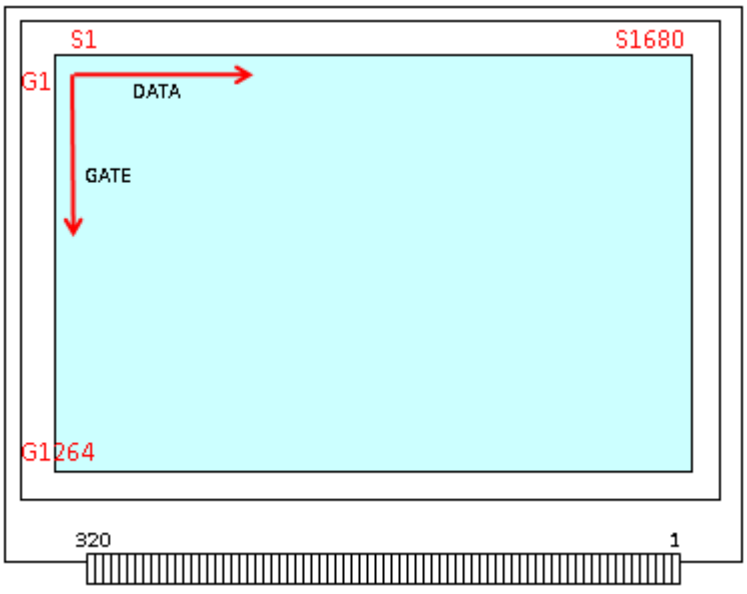
Connector type：FH34SRJ-45S-0.5SH (50)

Pin #	Signal	I/O	Description	Remark
1	VGL	P	Negative power supply gate driver	Note1
2	NC	-	No Connection	
3	VGH	P	Positive power supply gate driver	Note1
4	NC	-	No Connection	
5	VDD	P	Digital power supply drivers	Note1
6	OEV	I	Output mode selection gate driver	
7	CKV	I	Clock gate driver	
8	SPV	I	Start pulse gate driver	
9	NC	I	No Connection	
10	VCOM	P	Common voltage	Note1
11	NC	-	No Connection	
12	VCOM	P	Common voltage	Note1
13	NC	-	No Connection	
14	D0	I	Data signal source driver(LSB)	
15	D1	I	Data signal source driver	
16	D2	I	Data signal source driver	
17	D3	I	Data signal source driver	
18	D4	I	Data signal source driver	
19	D5	I	Data signal source driver	
20	D6	I	Data signal source driver	
21	D7	I	Data signal source driver	
22	VSS	P	Ground	Note1
23	CKH	I	Clock source driver	
24	VSS	P	Ground	Note1
25	D8	I	Data signal source driver	
26	D9	I	Data signal source driver	
27	D10	I	Data signal source driver	
28	D11	I	Data signal source driver	
29	D12	I	Data signal source driver	
30	D13	I	Data signal source driver	

31	D14	I	Data signal source driver	
32	D15	I	Data signal source driver(MSB)	
33	SPH	I	Start pulse source driver	
34	LEH	I	Latch enable source driver	
35	OEH	I	Output enable source driver	
36	XON	-	XON control for night mode (default pull high)	
37	NC	-	No Connection	
38	VCOM	P	Common voltage	Note1
39	NC	-	No Connection	
40	NC	-	No Connection	
41	VSH	P	Positive power supply source driver	Note1
42	NC	-	No Connection	
43	VSL	P	Negative power supply source driver	Note1
44	NC	-	No Connection	
45	Border	I	Border Connection	

Note1: P → Power pin

5.2 Panel Scan Direction



5.3 The relationship of input data and output

Output	S1	S2	S3	S4	S5	S6	S7	S8
Data	D15	D13	D11	D9	D7	D5	D3	D1
	D14	D12	D10	D8	D6	D4	D2	D0

5.4 Recommended Connector Type of Front Light

FH34SRJ-8S-0.5SH(50)

5.5 Pin assignment of LED circuit

No.	Pin assignment	Remark
1	Warm 1-	Warm 1 (11pcs LED)
2	Warm 1+	
3	dummy	
4	dummy	
5	Cool 1-	Cool 1 (12pcs LED)
6	Cool 1+	
7	dummy	
8	dummy	

5.6 Recommended Connector Type of Touch Panel

FH34SRJ-8S-0.5SH(50)

5.7 Pin Assignment of Touch Panel (Note.)

Pin#	Signal	I/O	Description	Remark
1	GND	P	Ground	Note.
2	NC	-	No Connection	
3	XRESET	I	Reset pin from mainboard to IC digital I/O by VDDIO	Already mounted pull high resistor 10K ohm for XRESET by touch FPC.
4	INT	I/O	Interrupt pin from IC to main board digital I/O by VDDIO	Already mounted pull high resistor 10K ohm for INT by touch FPC.
5	I2C_SDA	I/O	I2C data pin to ELAN touch IC digital I/O by VDDIO	Already mounted pull high resistor 2.2K ohm for SDA by touch FPC.
6	I2C_SCL	I/O	I2C clock pin to ELAN touch IC digital I/O by VDDIO	Already mounted pull high resistor 2.2K ohm for SCL by touch FPC.
7	VDDIO	P	Host supply 1.8V or 3.3V for digital I/O by main board input	Power supply for I/O pad
8	VDD_TP	P	Power supply DC 2.8V~3.4V (Ripple < ±200mV)	Note.

Note: P → Power pin

5.8 Touch panel Characteristics

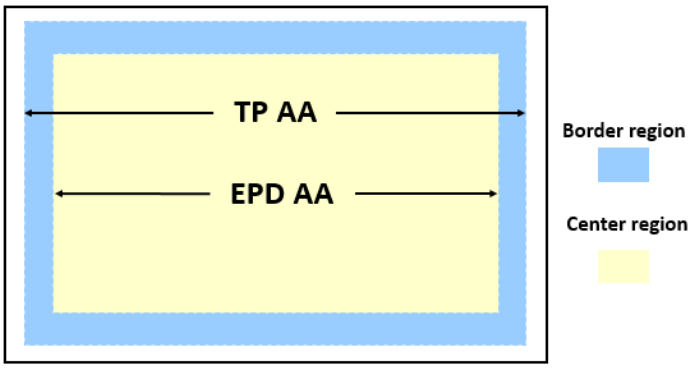
5.8.1 Touch Panel Performance by finger (Report Rate: 90 Hz)

Symbol		Specification	Remark
Finger diameter		7mm	
Linearity	Center	±1	No display refresh
	Border	±2	
Accuracy	Center	±1	No display refresh
	Border	±2	
Jitter	Center	±1	No display refresh
	Border	±2	
Water Rejection	(1) No false touch with small water droplet or condensation. (2) The touch will not be triggered by water when it's totally immersed.		No display refresh

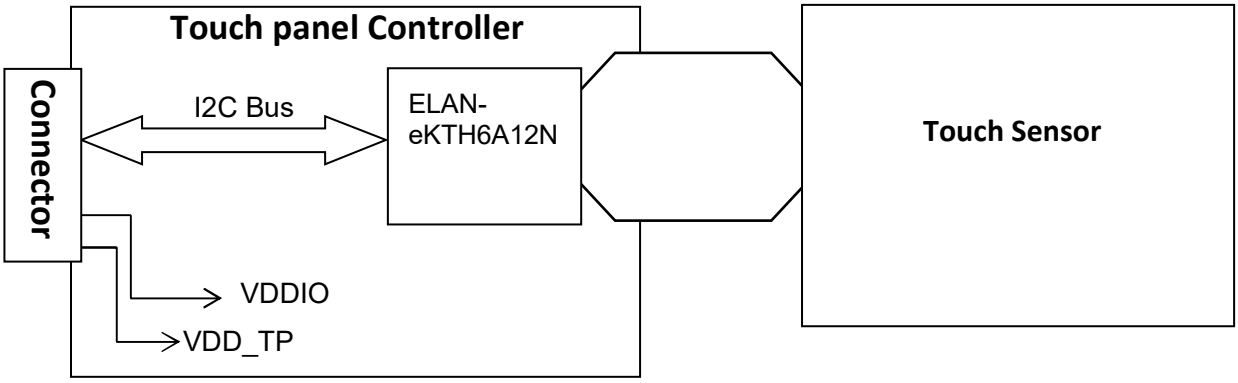
5.8.2 Touch Panel Performance by stylus (Note.)

Symbol	Specification	Remark
Stylus diameter	≧ 1.2 mm	Note.
Stylus accuracy [mm]	Center :+/- 0.6mm, Border +/- 1.25mm (follow TP IC test method)	No tilt Note.
Stylus linearity [mm]	Center: +/- 0.4mm, Border : +/- 0.8mm (follow TP IC test method)	No tilt Note.
Stylus report rate [Hz]	≦ 266Hz	Note.
Stylus response time (active mode)	< 20ms	Note.
Stylus response time (idle mode)	< 50ms	Note.
Power consumption (active mode)	40mA(ref. only)	Note.
Power consumption (idle mode)	15mA(ref. only)	Note.
Power consumption (sleep mode)	0.5mA(ref. only)	Note.
Pressure sensitivity	4096 levels	Note.
Hovering	5mm	
Tilt angle detection	No	Accuracy impact taken into consideration

Note: The final stylus specification will be come out base on device firmware fine tune lockdown setting.



5.8.3 Touch Panel circuit application



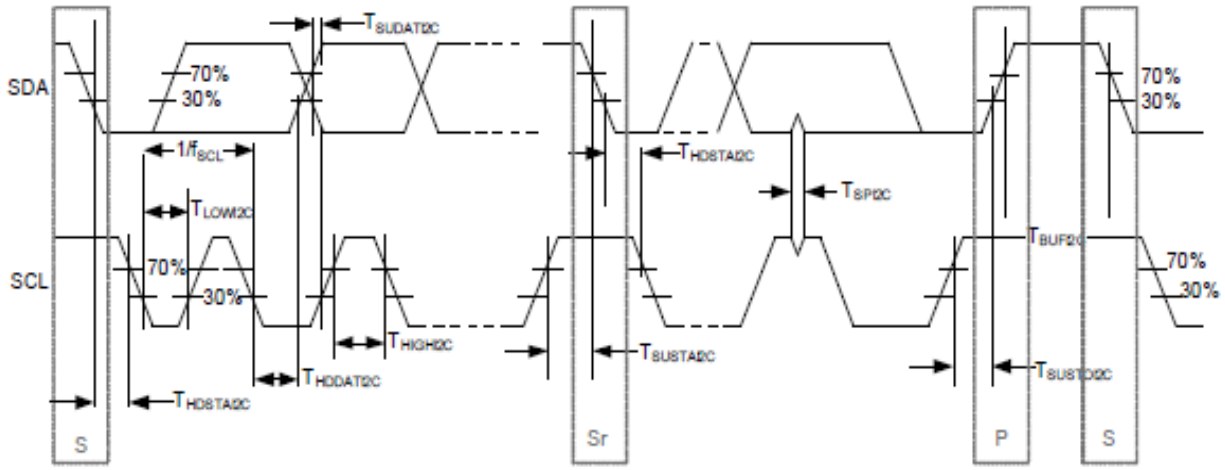
5.8.4 Touch driver IC DC Characteristics: (Note.)

Parameter	Pins	Symbol	Condition	Rated value			Unit
				Min.	Typ.	Max.	
Power supply voltage	Power	VDD_TP	-	2.8	3.3	3.4	V
	Power	VDDIO	-		1.8 3.3		
Normal mode Current consumption	Power	I_{Normal}	VDD_TP = 3.3V	-	40	-	mA
Idle mode Current consumption		I_{Idle}	VDD_TP = 3.3V	-	10	-	
Sleep mode Current consumption		I_{Sleep}	VDD_TP = 3.3V	-	0.5	-	

Note:

1. The final touch module consumption will be come out base on device firmware tune lockdown setting.
2. The power consumption is only for reference.

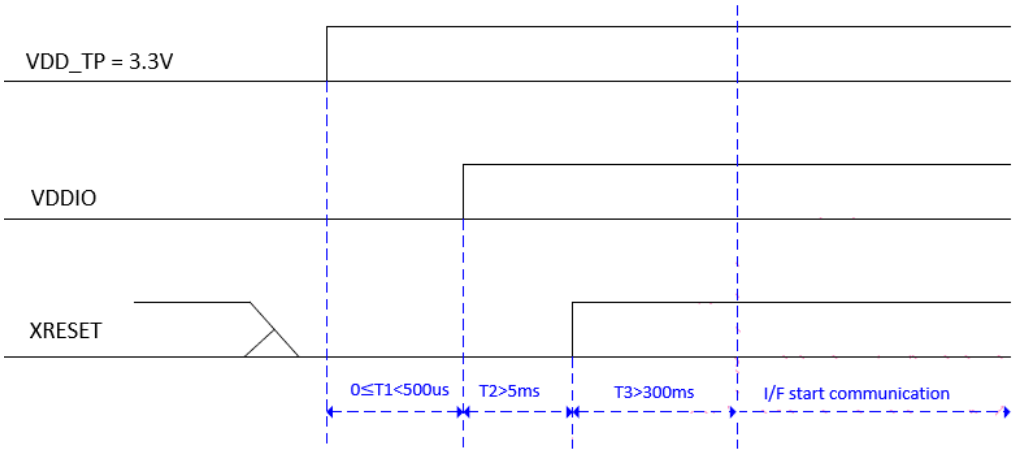
5.8.5 Touch driver IC I2C Bus Timing Diagram for Fast/Standard Mode



Legend
S: I²C Start Condition
Sr: I²C Repeat Start Condition
P: I²C Stop Condition

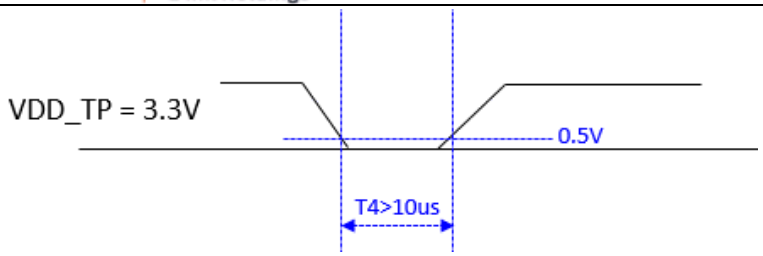
5.8.6 Touch driver IC Power Sequence: (Note.)

Power on sequence:



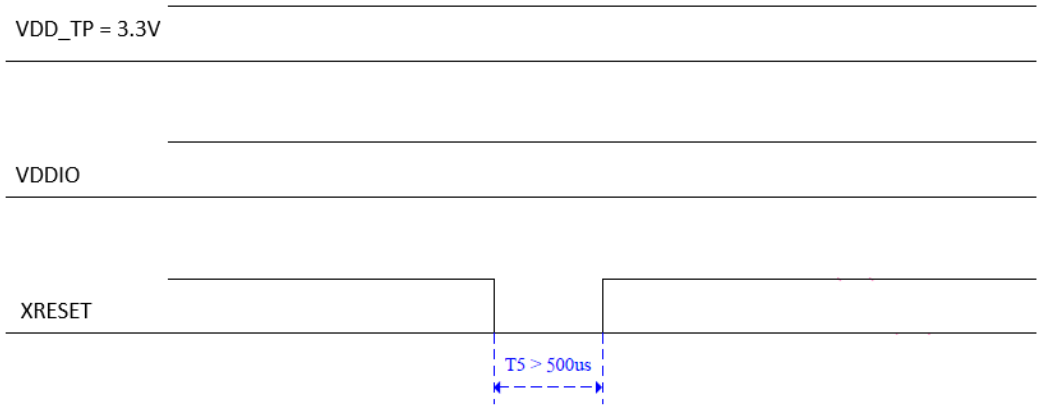
Note： I/F start communication must star after XRESET successfully 300ms.
The rising time of VDD_TP should be less than 1ms.
Power signal can’t ramp down during power rising cycle.

Power off sequence



Note：During power off, the VDD_TP must be less than 0.5V for at least 10us to make sure the touch controller is power off correctly.

XRESET sequence



Note：In case a user wants to reset the controller without powering off, pull low the reset for more than 500us.